## REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 through 20 remain in this case. Amendment to claims 1 through 3, 5, 7, 9, 12 through 14, 17 through 19, and 20 is presented.

Applicant proposes amending paragraph 119 of the specification to correct an error of a typographical nature, and to render this paragraph of the specification consistent with the remainder of the specification. The proposed specification amendment changes the sentence "The local memory may be positioned at a level other than L2." to now read "The local memory may be positioned at a level other than L1." Several other references in the specification to the local memories refer to the local memory as at level 1, or L1.[1] Further, the elements of the drawings to which the specification refers as "local memories" are clearly lower in level (*i.e.*, closer to the processors) than the shared memory and level 2 cache.[2] Applicant therefore respectfully submits that no new matter is presented by this amendment to the specification, and that this amendment is proper in correcting this typographical error.

Claims 12 through 17 were objected to because of an informality regarding the phrase "the address space". Applicant proposes amendment to claim 12 so that it now recites this phrase as "an address space", obviating the objection. Applicant submits that the amendment presented to claim 12, and thus to its dependent claims 13 through 17, is in no way narrowing nor is presented for any reason related to patentability,[3] and presents no new matter.

Claims 1, 2, and 5 were finally rejected under §103 as unpatentable over the Baron et al. reference[4] in view of the Tanenbaum reference[5]. The Examiner asserted that the Baron et al.

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[1] Specification of S.N. 09/932,381, paragraphs 05 and 06 on page 8; paragraph 17 on page 12.
[2] S.N. 09/932,381, *supra*, Figures 1, 2A, and 2B.
[3] *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 535 U.S. 722, 62 USPQ2d 1705 (2002), *on remand*, 304 F.3d 1289, 64 USPQ2d 1698 (Fed. Cir. 2002).
[4] U.S. Patent No. 5,586,293, issued December 17, 1996 to Baron et al.

reference teaches all of the elements of claim 1 except for the specifics of the DMA transfer, which the Examiner found to be taught by Tanenbaum; the Examiner further asserted that the skilled artisan would have obviously combined the DMA transfer operation from Tanenbaum into the Baron et al. system to free the CPU from low-level work.[6] Claim 11 was also finally rejected under §103 as unpatentable over the Nakagawa et al. reference[7], in view of the combination of the Baron et al. and Tanenbaum references.[8]

Applicant respectfully traverses the §103 rejection of claim 11, on the grounds that the cited Nakagawa et al. reference is not prior art to this application. The filing date of this application is August 17, 2001, with priority claimed back to August 21, 2000. The Nakagawa et al. reference has an issue date of November 4, 2003, which is clearly after the filing date of this application, and therefore negates its availability under any of §102(a), §102(b), and §102(d). The filing date of the Nakagawa et al. reference is December 28, 2001, which is also after both the filing date and the priority date of this application, negating its availability under §102(e). While the Nakagawa et al. reference claims priority to an earlier filed U.S. application[9], this earlier filed application and its resulting issued patent is not cited against the claim. Applicant therefore respectfully traverses the final rejection of claim 11, on the grounds that the primary reference applied by the Examiner is not prior art to the claim.

Amendment is also presented to claim 1 to overcome the §103 rejection.

Claim 1 requires, *inter alia*, a local memory that occupies a portion of the address space of the at least first processor, comprising a data array arranged as a plurality of segments and a plurality of indicator bits, and DMA circuitry that is operable to transfer data to a selectable portion of segments of the local memory and that is operable to manipulate a selected portion of the indicator bits corresponding to the selectable portion of segments. Claim 2 further recites, relative to claim 1 upon which it depends, that the plurality of indicator bits are valid bits, set

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[5] Tanenbaum, *Modern Operating Systems* (Prentice-Hall, 1992), pp. 208-10.
[6] Office Action of December 13, 2002, pages 4 and 5, ¶7.
[7] U.S. Patent No. 6,643,713 B2, issued November 4, 2003 to Nakagawa et al.
[8] Office Action, *supra*, pages 5 and 6, ¶8.

by the DMA circuitry to a valid state corresponding to the selectable portion of segments. Proposed amended claim 1 now further recites address circuitry for controlling access by the first processor to an addressed location of the local memory within the address space and responsive to the state of the indicator bits corresponding to the addressed location. The specification clearly supports this additional element to claim 1,[10] and as such no new matter is presented by this amendment. Claim 2 is amended to now further recite that the address circuitry permits access by the first processor to the addressed location responsive to the corresponding indicator bits being in the valid state.[11]

The digital system of proposed amended claims 1 and 2, and dependent claim 11, provide important advantages in modern digital systems. In particular, this system provides the important advantages of providing a local memory for a processor, especially in a multiple-processor system, in which data may be transferred to the local memory by DMA, and in which processor and DMA access to the local memory can be readily coordinated.

Applicant respectfully submits that the Baron et al. and Tanenbaum references fail to teach the address circuitry and its function in controlling access by the first processor responsive to the state of the indicator bits, as required by the claims. The Examiner asserted that the Baron et al. reference teaches that the RAM 10 of the Baron et al. reference can operate in a "PRAM mode" (program memory mode), and that the valid bits of this RAM are set by a DMA transfer.[12] But this cited location teaches only that the state of these valid bits of RAM 10 in PRAM mode is only pertinent with the CACHE MODE of RAM 10.[13] Reading a bit further in the Baron et al. reference from the cited portion, one learns that "[t]he valid bits are not tested and the HIT/MISS_ signal is ignored".[14] Accordingly, when RAM 10 is operating as a local memory within the address space of its processor, there is no use of the valid bits. Accordingly, the reference fails to disclose the controlling of access by the first processor to an addressed

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[9] Application S.N. 09/051,286, filed as a PCT application PCT/JP96/02910, and now U.S. Patent No. 6,353,863.
[10] Specification, *supra*, paragraphs 84 and 85, page 30.
[11] *Id.*
[12] Office Action, *supra*, page 4, ¶7, *citing* Baron et al., *supra*, at column 8, lines 31 through 35.
[13] Baron et al., *supra*, column 8, lines 31 through 35.

location of the local memory within the address space and responsive to the state of the indicator bits corresponding to the addressed location, and therefore fails to disclose the address circuitry of proposed amended claim 1. The Tanenbaum reference fails to add any teachings to the Baron et al. reference in this regard, and therefore Applicant respectfully submits that the combined teachings of the applied references fall short of the requirements of proposed amended claims 1 and 2.

Applicant further respectfully submits that there is no suggestion to modify these teachings in such a manner as to reach the requirements of claims 1 and 2. There is no such suggestion from the Baron et al. and Tanenbaum references to utilize the indicator bits in local memory access by the processor; rather, as noted above, the Baron et al. reference expressly states that the valid bits are not tested in the PRAM mode. The other references applied against the other claims in this case add no teachings in this regard. Further, there is no suggestion from any of these references regarding a local processor memory to which DMA transfers can be made and to which the processor can access the local memory responsive to the valid bits set by the DMA, as claimed, much less suggestion of the important advantages provided by the claimed system.

Applicant therefore respectfully submits that proposed amended claims 1 and 2, and dependent claim 11, are patentably distinct over the applied references. Entry of the amendment to these claims, and their favorable reconsideration, are respectfully requested.

Claims 3, 4, and 6 through 10, were objected to as dependent upon a rejected base claim, but were indicated as directed to allowable subject matter.[15]

Claim 3 is proposed to be amended to be presented in independent form, incorporating the limitations of claims 1 and 2 upon which it previously depended, as suggested by the Examiner. Claim 5 is also proposed to be amended to now depend upon proposed amended claim 3, and for consistency with this new dependency, obviating the §103 rejection to claim 5.

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[14] Baron et al., *supra*, column 8, lines 36 through 39.
[15] Office Action, *supra*, pages 8 and 9, ¶¶ 10 and 11.

Claim 7 is also proposed to be proposed to be amended to be presented in independent form, incorporating the limitations of claim 1 upon which it previously depended.

Claim 9 is proposed to be amended for clarity, now reciting that the first dirty bit is operable to be reset in response to a write transaction by the DMA circuitry. Applicant submits that the specification clearly supports the proposed amendment to claim 9,[16] and that therefore no new matter is presented.

Applicant further submits that this proposed amendment to claims 3, 7, and 9 do not narrow the scope of any of these claims, and is not presented for any reason related to patentability.[17]

Applicant therefore respectfully submits that, upon entry of this amendment, claims 3 through 10 will be in condition for allowance.

Claims 12 and 17 through 19 were rejected under §102(b) as anticipated by the Blumrich et al. reference[18]. The Examiner asserted that memory 8 of the reference corresponds to the local memory of the claim, which is organized by a memory management unit into a plurality of page tables (corresponding to segments); the Examiner further asserted that the reference teaches a dirty bit for pages, which is marked as dirty if written by an incoming DMA operation.[19] The claims were rejected accordingly, and the rejection was made final.

Claims 12 and 13 were also finally rejected under §103 as unpatentable over the Baron et al. reference in view of the Tanenbaum reference, on a similar basis as discussed above relative to claim 1.

Claim 12 is proposed to be amended to overcome the rejections. The method of proposed amended claim 12 now further requires the step of controlling access by the processor to the first segment in the local memory within the address space, responsive to the state of the

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[16] Specification, *supra*, paragraph 101, page 34.
[17] *See Festo, supra.*
[18] U.S. Patent No. 5,659,798, issued August 19, 1997, to Blumrich et al.
[19] Office Action, *supra*, page 3, ¶5.

first indicator bit. The specification clearly supports this additional element to claim 12,[20] and as such no new matter is presented by this amendment. The method of proposed amended claim 12 provides the important advantages discussed above relative to proposed amended claim 1.

Claim 13 is also proposed to be amended, by now reciting that the controlling step permits access by the processor to the first segment responsive to the corresponding indicator bits being in the valid state.[21]

Applicant respectfully submits that proposed amended claims 12 and 13 are novel and patentably distinct over the applied references.

The Blumrich et al. reference fails to disclose the controlling step of proposed amended claim 12. First, the reference fails to disclose the step of organizing a local memory, because the reference fails to disclose the presence of a local memory. Figure 3 of the Blumrich et al. clearly shows that memory 8 is not local to CPU 4; rather, the CPU 4 is shown as addressing memory 8 only through the UDMA hardware 44 and DMA controller 2.[22] The text of the reference is consistent with memory 8 not being a local memory, as it teaches that its "UDMA Hardware 40 is situated between the standard DMA controller 2 and the CPU 4"[23], and that this hardware effects address translation from the physical address on the CPU address bus 46 to the "physical proxy address" that is applied to memory 8 in a DMA transfer.[24] Applicant therefore respectfully submits that memory 8 of the reference is in no way a "local memory" to a processor, especially considering the address translation as required in order for the CPU to access this memory, and that therefore the organizing step of claim 12 is not met by the reference.

Further, Applicant respectfully submits that the Blumrich et al. reference fails to disclose the controlling step of claim 12, because it nowhere discloses the responsive access of its memory by the processor in response to the state of the indicator bits. Instead, the alleged

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[20] Specification, *supra*, paragraphs 84 and 85, page 30.
[21] *Id.*
[22] Blumrich et al., *supra*, Figure 3.
[23] Blumrich et al., *supra*, column 11, lines 18 and 19.
[24] Blumrich et al., *supra*, column 11, lines 23 through 28.

indicator bits of the Blumrich et al. reference are disclosed only as indicating whether the "dirty" pages are to be written to backing store, for coherency purposes.[25]

As discussed above relative to proposed amended claim 1, Applicant further respectfully submits that the Baron et al. and Tanenbaum references fail to teach the step of controlling access by the processor responsive to the state of the first indicator bit, as required by proposed amended claims 12 and 13. As discussed above, the Baron et al. reference expressly states that its "[t]he valid bits are not tested and the HIT/MISS_ signal is ignored" when its memory is in "PRAM mode".[26] The reference therefore fails to disclose the controlling of access by a processor to a local memory within its address space responsive to the state of an indicator bit, as required by proposed amended claim 12. The Tanenbaum reference fails to add any teachings to the Baron et al. reference in this regard. Applicant therefore respectfully submits that the combined teachings of the applied references fall short of the requirements of proposed amended claims 12 and 13.

Applicant further respectfully submits that there is no suggestion to modify these teachings in such a manner as to reach the requirements of these claims. None of the references suggest utilize the indicator bits to control local memory access by the processor. The other references of record also add no teachings in this regard. The important advantages provided by the claimed method also support the importance, and thus the patentability, of these claims.

Applicant therefore respectfully submits that proposed amended claims 12 and 13 are novel and patentably distinct over the applied references. Entry of the amendment to these claims, and their favorable reconsideration, are respectfully requested.

Claims 14 through 16 were objected to as depending on a rejected claim, but were indicated as allowable if represented in independent form, incorporating the limitations of their base claims.[27]

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[25] Blumrich et al., *supra*, column 16, lines 52 through 60.
[26] Baron et al., *supra*, column 8, lines 36 through 39.
[27] Office Action, *supra*, pages 8 and 9, ¶¶ 10 and 11.

Claim 14 is proposed to be amended as suggested by the Examiner, incorporating thereinto the limitations of previous claims 12 and 13. Applicant submits that this proposed amendment to claim 14 does not narrow the scope of this claim, and is not presented for any reason related to patentability.[28]

Claim 17 (previously finally rejected under §102), is also proposed to be amended to now depend on claim 14, obviating the rejection to it and claims 18 and 20 which depend on claim 17. Claim 18 is proposed to be amended for consistency with proposed amended claim 17, upon which it depends.

Claim 19 is also proposed to be amended, for clarity, by now reciting the step of resetting the first dirty bit in response to a DMA write transaction to the first segment associated with that first dirty bit. Applicant submits that the specification clearly supports the proposed amendment to claim 19,[29] and that therefore no new matter is presented.

Applicant therefore respectfully submits that proposed amended claim 14, and its dependent claims 15 through 20 (as proposed to be amended), will all be in condition for allowance upon entry of this amendment.

For the reasons discussed above, Applicant submits that, upon entry of this amendment, all claims in this case will be in condition for allowance. Alternatively, Applicant submits that this amendment to the claims places this case in better condition for appeal.

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[28] *See Festo, supra.*

[29] Specification, *supra*, paragraph 101, page 34.

Accordingly, Applicant respectfully requests entry of this amendment, and reconsideration of this application.

Respectfully submitted,

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